ABSTRACT

Multiple streams of bits are received. One or more bits are selected from a stream of bits based, at least in part, on a space control register value and a time control register value. In one embodiment, a time control register stores a value indicating a selected bit from a sequence of bits, a counter counts bits in the sequence of bits from a predetermined bit, and a comparator is coupled to the time control register and to the counter to generate a load signal when a value stored in the time control register and a value provided by the counter are equal. The load signal causes the latch to load a value output by the multiplexer.